CHARLES DARWIN UNIVERSITY

Family Name	
Given Names	
Student Number	
Teaching Period	Semester 1, 2017

FINAL EXAMINATION	**DURATION**
HIT235 – Digital Systems and Computer Architecture	Reading Time: **10** minutes Writing Time: **180** minutes

INSTRUCTIONS TO CANDIDATES

The examination has one section.

Note that questions ARE NOT of equal value.

Read ALL questions carefully.

Answer ALL questions.

EXAM CONDITIONS

You may begin writing from the commencement of the examination session. The reading time indicated above is provided as a guide only.

This is a CLOSED BOOK examination

Any non-programmable calculator is permitted

No handwritten notes are permitted

No dictionaries are permitted

ADDITIONAL AUTHORISED MATERIALS	EXAMINATION MATERIALS TO BE SUPPLIED
none	1 x 20 Page Book 1 x Scrap Paper

THIS EXAMINATION IS PRINTED DOUBLE-SIDED.

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Question 1 (4 marks)

A bush fire risk detection system is required. The bush fire risk depends on several variables of which the humidity, temperature and wind speed are the main ones. When the humidity is high, a green light should be on, indicating a low risk. If the humidity is low but the temperature and wind speed are also low, there is a moderate risk and an orange light should be on. If the humidity is low and the temperature is high there is a high risk of a bush fire and a red light should be on. The red light should also be on if the humidity is low and the wind speed is high. If the humidity is low and both the temperature and the wind speed are high the bush fire risk is extreme a "Total Fire Ban" sign should be switched on. Design the logic circuit for this system.

Question 2 (2 marks)

What is the advantage of using binary code instead of BCD code?

Question 3 (4 marks)

a) Give the truth table for a full adder. (2 mark)
b) How many gates do you need to make a full adder? Explain your answer. (2 marks)

Question 4 (3 marks)

What is the difference between the propagation delay time and the set up time of a flip-flop?

Question 5 (4 marks)

Each of the eight full-adders in an 8-bit parallel ripple carry adder exhibits the following propagation delays:

A to Sum (Σ) and $Carry_{out}$	15 ns
B to Sum (Σ) and $Carry_{out}$	15 ns
$Carry_{in}$ to Sum (Σ)	30 ns
$Carry_{in}$ to $Carry_{out}$	25 ns

Determine the maximum total time for the addition of two 8-bit numbers.

Question 6 (4 marks)

a) Give the truth table of an XNOR gate (1 mark)
b) Is it possible to implement an XNOR gate, using only NOR gates? If no, explain why not. If yes, draw the circuit. (3 marks)

Question 7 (3 marks)

For the cascade counter shown in Figure 1, the input frequency is 400 kHz. Determine the frequency of the waveform at each point indicated by a circled number.

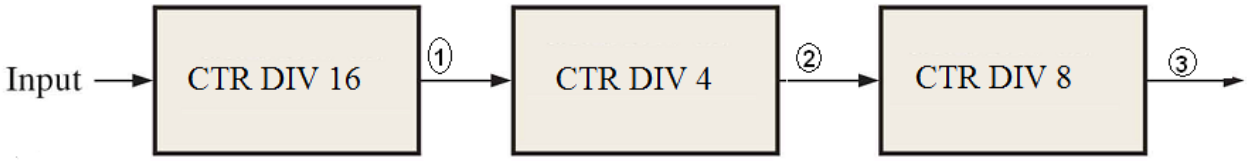

Figure 1

Question 8 (3 marks)

Explain how addition of negative binary numbers can be done.

Question 9 (4 marks)

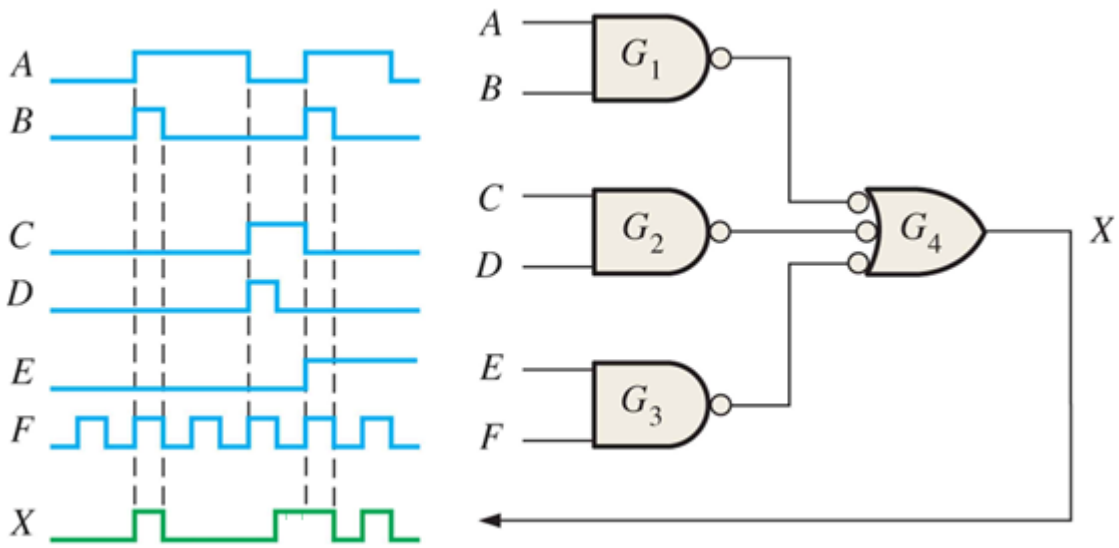

Figure 2

a) The output waveform shown above is not correct. Draw the correct waveform. (2 marks)
b) The output waveform is the result of incorrect implementation of the circuit. One of the gates has been replaced by another type of gate. Which gate has been replaced and what is the replacement gate? Explain your answer. (2 marks)

Question 10 (4 marks)

Apply De Morgan's theorems and the rules of Boolean algebra to simplify the following expressions:

a) $\overline{\overline{A}B(\overline{C}D + \overline{BE})(A\overline{B} + B\overline{C}D)}$ (2 marks)

b) $\overline{(\overline{A} + \overline{B})}\ \overline{(B + D)}\ \overline{(\overline{A} + \overline{C})}\ \overline{(\overline{A} + B)}$ (2 marks)

Question 11 (6 marks)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 1

For the truth table shown above,
a) Derive the standard Sum Of Product (SOP) and the standard Product Of Sums (POS) expression. (3 marks)
b) Use a Karnaugh map to find the minimum SOP expression. (3 marks)

Question 12 (4 marks)

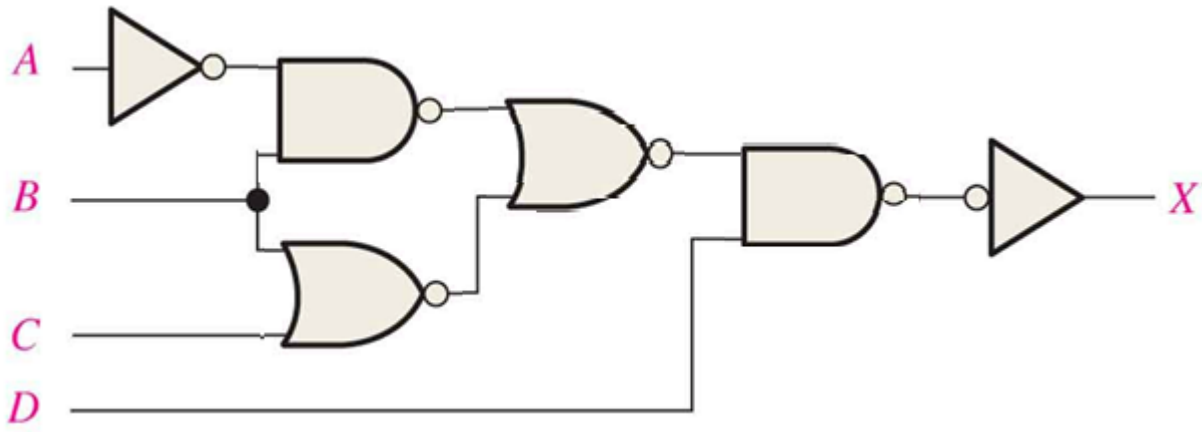

Figure 3

For the circuit shown in Figure 3, determine the output equation. Is it possible to implement the circuit using fewer gates? If yes, draw the circuit.

Question 13 (3 marks)

Can a J-K flip-flop be modified to create a D flip-flop? If no, explain why not. If yes, explain how.

Question 14 (3 marks)

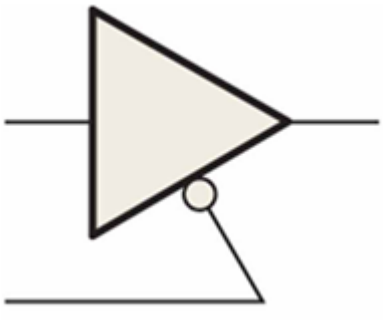

Figure 4

Is the element shown in Figure 4 a tri-state inverter? Explain your answer.

Question 15 (4 marks)

Draw the circuit diagram of a circuit that gives a HIGH output when 2 bit number *B* is larger or equal than 2 bit number *A*.

Question 16 (5 marks)

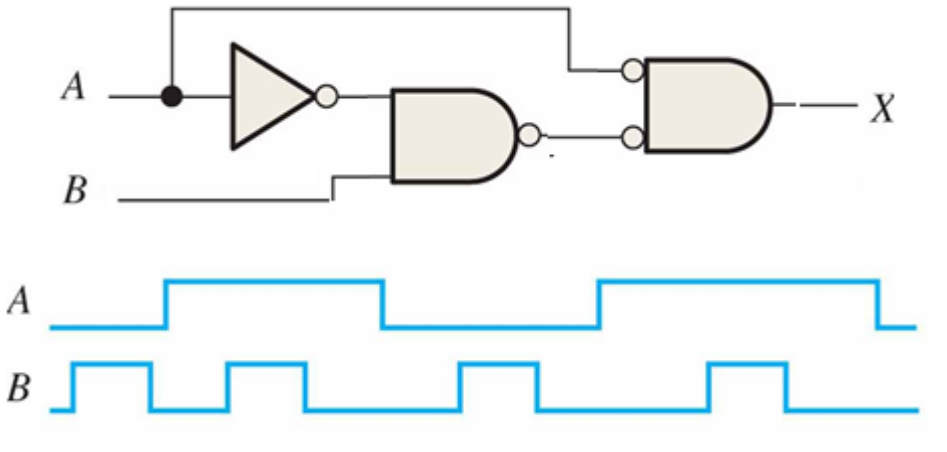

Figure 5

a) Determine the output expression for the circuit shown in Figure 5. (2 marks)
b) Draw a timing diagram for the circuit shown in Figure 5, showing the output in the proper relationship with the input signals. (3 marks)

Question 17 (4 marks)

a) What is the difference between an astable multi-vibrator and a monostable multi-vibrator? (2 marks)
b) Give an application for each of them. (2 marks)

Question 18 (3 marks)

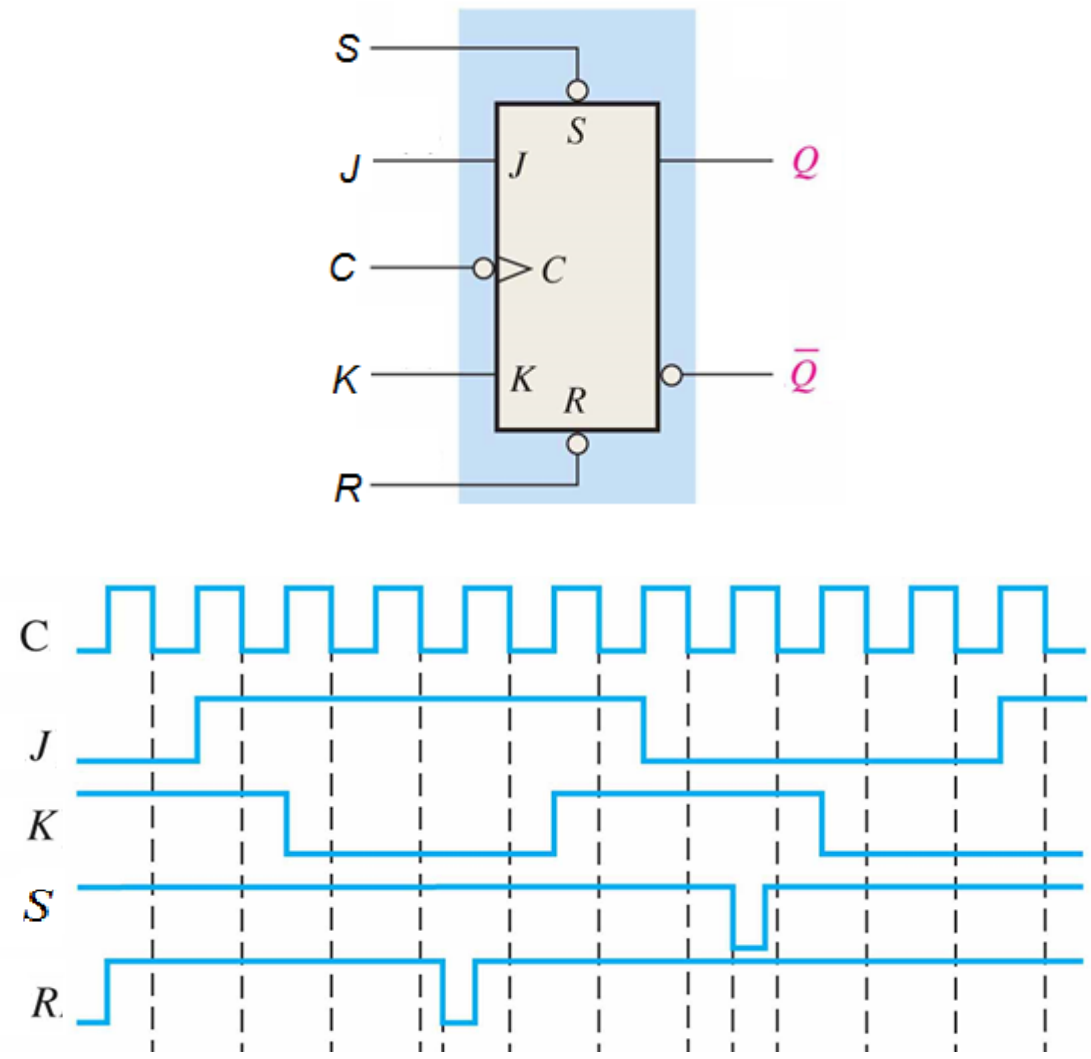

Figure 6

For the inputs and the circuit shown in Figure 6, determine the *Q* output. Assume the *Q* output is initially low.

Question 19 (4 marks)

Design a digital circuit, using several *J-K* flip-flops and some logic gates to create a digital counter which counts from 0 to 6 and then starts again at 0.

Question 20 (2 marks)

Give two examples of weighted number systems.

Question 21 (3 marks)

What is the function of a decoder? Give a practical application of a decoder.

Question 22 (3 marks)

What is the function of the circuit shown in Figure 7?

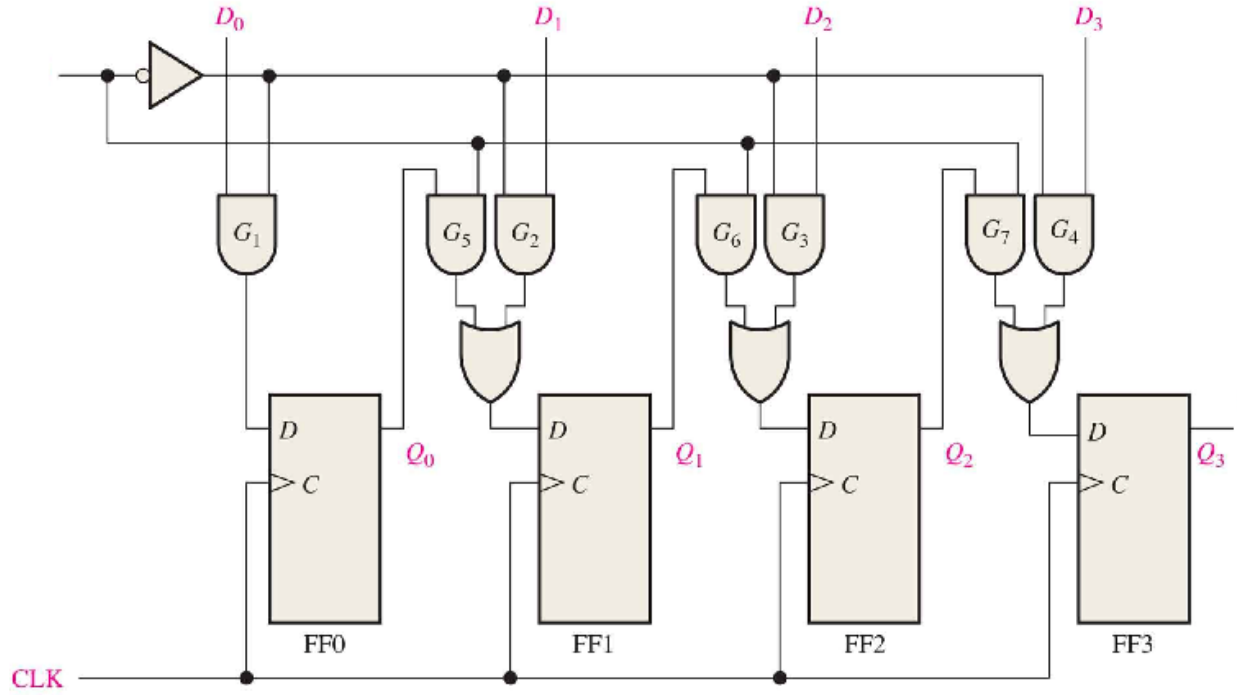

Figure 7

Question 23 (3 marks)

Please answer with yes or no for each subquestion. Is a dual core processor required for
a) Pipelining (1 mark)
b) Multitasking (1 mark)
c) Multithreading (1 mark)

Question 24 (3 marks)

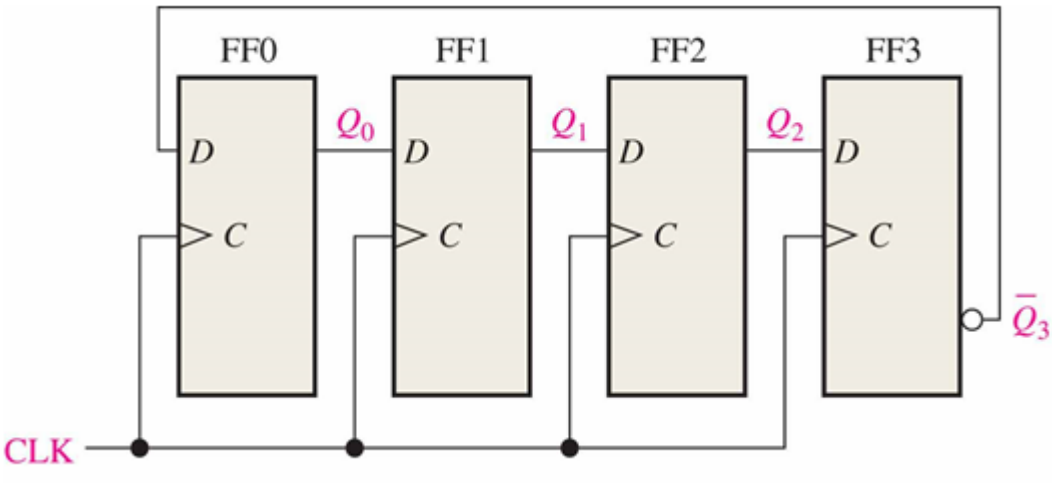

Figure 8

What is the circuit shown in Figure 8 called and what is its function?

Question 25 (4 marks)

Form the 2's complement of the following numbers:

a) 11111011 (2 marks)
b) 10101111 (2 marks)

Question 26 (3 marks)

What is the relevance of propagation delays for the design of digital circuits?

Question 27 (2 marks)

What is the function of:

a) the address bus (1 mark)
b) the ALU (1 mark)

Question 28 (3 marks)

Explain how you could design a circuit that subtracts one 3 bit number from another 3 bit number.

Question 29 (3 marks)

Is it possible to build a circuit that performs the same function as the circuit shown in Figure 9 using only *JK* flip-flops? Explain your answer.

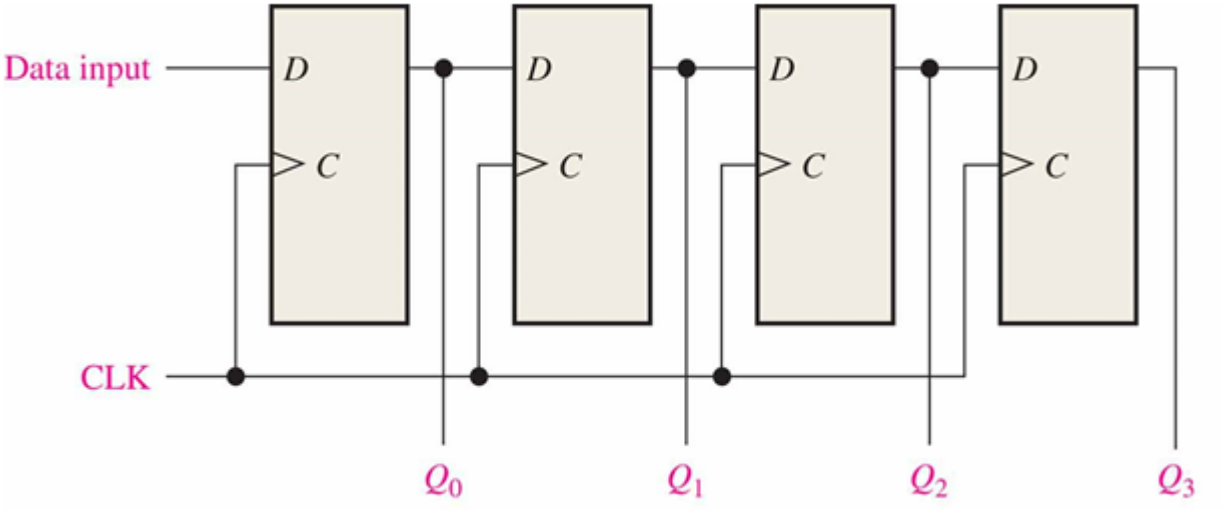

Figure 9